Suwan Kim

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Research Interests

Focused on **Electronic Design Automation**, with specific interests in, but not limited to:

- AI-aided design automation
- Design and technology co-optimization (DTCO)
- Design methodologies for advanced technology

Education

- **Seoul National University** — Seoul, Korea
  Ph.D. in Electrical and Computer Engineering — Sep. 2019 - Aug. 2024
  - Advisor: Prof. Taewhan Kim
  - Dissertation: *"Methodologies of Utilizing Design Enablement Resources for High-Quality Physical Design"*

- **Seoul National University** — Seoul, Korea
  B.S. in Electrical and Computer Engineering — Mar. 2013 - Aug. 2019
  B.S. in Naval Architecture and Ocean Engineering — Mar. 2013 - Aug. 2019

Experience

- **Kyung Hee University** — Suwon, Korea
  Assistant professor, Department of Semiconductor Engineering — Sep. 2025 - Present

- **AI Center, Samsung Electronics** — Suwon, Korea
  (previously AI Research Center, Samsung Advanced Institute of Technology) — Sep. 2024 - Aug. 2025
  Staff Engineer
  - Developed a DTCO methodology using Bayesian optimization for Samsung D1-delta DRAM standard cells.
  - Developed analog circuit parameter optimization framework using neural networks.

- **Samsung System LSI** — Suwon, Korea
  Research Intern — Nov. 2022 - Dec. 2022
  - Implemented a reinforcement learning-based macro placer on industrial designs, evaluating its impact on design quality.

Publications

International Journals

[J1] **Suwan Kim** and Taewhan Kim
"CFET-FP: Complementary FET Standard Cell Synthesis with Optimal Transistor Folding and Placement for Design and Technology Co-optimization"
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems ***(TCAD)*** (Accepted.)

[J2] **Suwan Kim** and Taewhan Kim.
"Design and Utilization of Multi-skewed Multi-bit Flip-flop Cells for Timing Optimization: Design and Technology Co-optimization"
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems ***(TCAD)***, Mar. 2025.

[J3] Hyunbum Park, Kyeonghyeon Baek, **Suwan Kim**, Kyumyung Choi, and Taewhan Kim.
"Pin Accessibility and Routing Congestion Aware DRC Hotspot Prediction for Designs in Advanced Technology Nodes With Consolidated Practical Applicability and Sustainability."
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems ***(TCAD)***, Dec. 2024.

[J4] **Suwan Kim** and Heechun Park
"Comprehensive Physical Design Flow Incorporating 3D Connections for Monolithic 3D ICs."
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems ***(TCAD)***, Jul. 2024.

International Conferences

[C1] Taejin Paik and **Suwan Kim**.
"HyperAnalog: Domain-Aware Hypergraph Transformer for Analog Circuit Representation Learning"
IEEE/ACM Design Automation Conference ***(DAC)***, July. 2026.

[C2] Youngmin Oh, Jinje Park, Taejin Paik, Seunggeun Kim, **Suwan Kim**, Yoon Hyeok Lee, and David Z. Pan
"M3: Mamba-assisted Multi-Circuit Optimization via Model-based RL with Effective Scheduling"
IEEE/ACM International Conference on Computer-Aided Design ***(ICCAD)***, 2025.

[C3] Cheng-Yu Tsai, **Suwan Kim**, and Sung Kyu Lim
"Capacitance Extraction via Machine Learning with Application to Interconnect Geometry Exploration"
IEEE/ACM International Conference on Computer-Aided Design ***(ICCAD)***, 2025.

[C4] **Suwan Kim** and Taewhan Kim.
"Optimal Transistor Folding and Placement for Synthesizing Standard Cells of Complementary FET Technology"
IEEE/ACM Design Automation Conference ***(DAC)***, Jun. 2024.

[C5] **Suwan Kim**, Hyunbum Park, Kyeonghyeon Baek, Kyumyung Choi, and Taewhan Kim.
"Methodology of Resolving Design Rule Checking Violations Coupled with Fully Compatible Prediction Model."
ACM International Symposium on Physical Design ***(ISPD)***, Mar. 2024.
(Acceptance rate: 18/62 = 29.0%)

[C6] **Suwan Kim** and Taewhan Kim.
"Design and Technology Co-optimization for Useful Skew Scheduling on Multi-bit Flip-flops"
IEEE/ACM International Conference on Computer-Aided Design ***(ICCAD)***, Oct. 2023.

[C7] Kyeonghyeon Baek, Hyunbum Park, **Suwan Kim**, Kyumyung Choi, and Taewhan Kim.
"Pin Accessibility and Routing Congestion Aware DRC Hotspot Prediction using Graph Neural Network and U-Net"
IEEE/ACM International Conference on Computer-Aided Design ***(ICCAD)***, Oct. 2022.

[C8] **Suwan Kim**, Sehyeon Chung, Taewhan Kim, and Heechun Park.
"Tightly Linking 3D via Allocation towards Routing Optimization for Monolithic 3D ICs"

IEEE/ACM International Symposium on Low Power Electronics and Design ***(ISLPED)***, Aug. 2022.

[C9] **Suwan Kim** and Taewhan Kim.
"Pin Accessibility-driven Placement Optimization with Accurate and Comprehensive Prediction Model"
IEEE/ACM Design, Automation and Test in Europe Conference ***(DATE)***, Mar. 2022.

[C10] **Suwan Kim** and Taewhan Kim.
"Practical Approach to Cell Replacement for Resolving Pin Inaccessibility"
IEEE Midwest Symposium on Circuits and Systems ***(MWSCAS)***, Aug. 2021.

[C11] **Suwan Kim**, Kyeongrok Jo, and Taewhan Kim.
"Boosting Pin Accessibility Through Cell Layout Topology Diversification"
IEEE Asia and South Pacific Design Automation Conference ***(ASP-DAC)***, Jan. 2021.

Domestic Conferences

[C1] **Suwan Kim** and Taewhan Kim
"Timing Improvement through Cell Replacement at ECO Routing"
Autumn Annual Conference of Institute of Electronics and Information Engineers ***(IEIE)***, Jan. 2021.

Patent

[P1] (Under registration) **Suwan Kim** and Taewhan Kim, "Apparatus of Multi-bit Flip-flop Circuit", Application number: 10-2024-0021068.

Awards & Fellowship

- **Distinguished Dissertation Award**, Department of ECE, SNU — Aug. 2024
- **Graduate Fellowship**, Samsung Advanced Institute of Technology — Sep. 2023

Academic Activity

- **Web Publicity Co-chair**, IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2024

Invited Talk

- **Standard cells, simple yet powerful design enablements**, Korean Conference on Semiconductors (KCS), South Korea, Feb. 2025

Projects

- **Development of Standard Cell Layout and Corresponding DTCO for PPA Optimization in Advanced Technology** — Jan. 2023 - Dec. 2023
  Samsung Electronics
  - Developed multi-bit flip-flop with various internal skew and corresponding DTCO methodology.
  Related works: ICCAD'23 [C6]

- **Software Systems for AI Semiconductor Design** Apr. 2021 - Dec. 2024
  Institute of Information & Communications Technology Planning & Evaluation (IITP)
  - Developed software for predicting and optimizing design rule violations at the pre-route stage.
  Related works: ICCAD'22 [C7], ISPD'24 [C5]

- **Deep Submicron Standard Cell Design** Mar. 2021 - Feb. 2026
  National Research Foundation of Korea (NRF)
  - Developed complementary-FET standard cell layout generator.
  Related works: DAC'24 [C4]

- **Development of Techniques for Overcoming Design and Verification Difficulties in Ultra Deep-Submicron Technology** Jul. 2020 - Feb. 2023
  National Research Foundation of Korea (NRF)
  - Developed a framework for generating standard cell layouts with various I/O pin accessibility and corresponding DTCO methodology.
  Related works: ASPDAC'21 [C11], MWSCAS'21 [C10]

- **Development of Physical Design Methodologies for Sub-14nm Technology** Sep. 2019 - Feb. 2021
  Seoul National University R&DB Foundation
  - Pin accessibility exploration by cell layout generation for mitigating routing complexity.
  Related works: ASPDAC'21 [C11]

Education Experience

Teaching

- Digital Circuit Design and Language, Kyung Hee University Sep. 2025
- Internal Instructor: CMOS VLSI Design, Samsung AI Center Apr. 2025
  - Taught core concepts in digital VLSI circuit design to AI researchers within my team.

Assistanships

- Logic Design for System Architect, Samsung Device Solution Feb. 2023, Feb. 2024
- Introduction to Algorithms, Seoul National University Fall 2020, Fall 2021, Fall 2023
- Digital Computer Concept and Practice, Seoul National University Spring 2022
- Digital Logic Design and Lab, Seoul National University Winter 2019

Miscellaneous

Military Service: Auxiliary Police at the Seoul Metropolitan Police Agency Oct. 2014 - Jul. 2016